National Research Tomsk State University

NICA SPD L2 concentrator firmware

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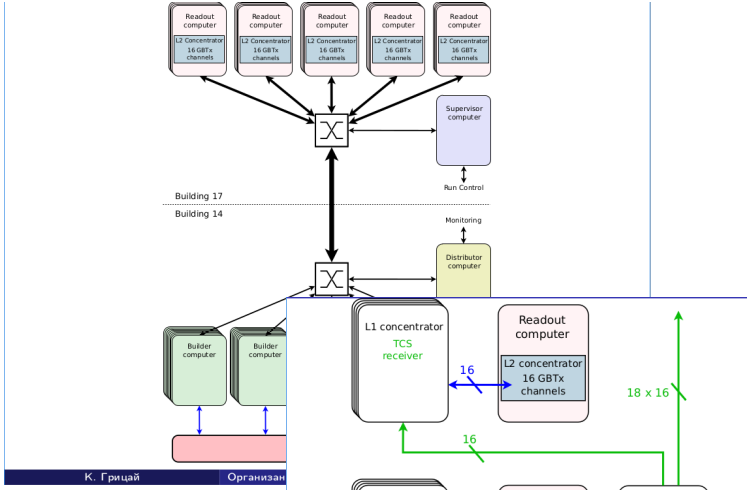
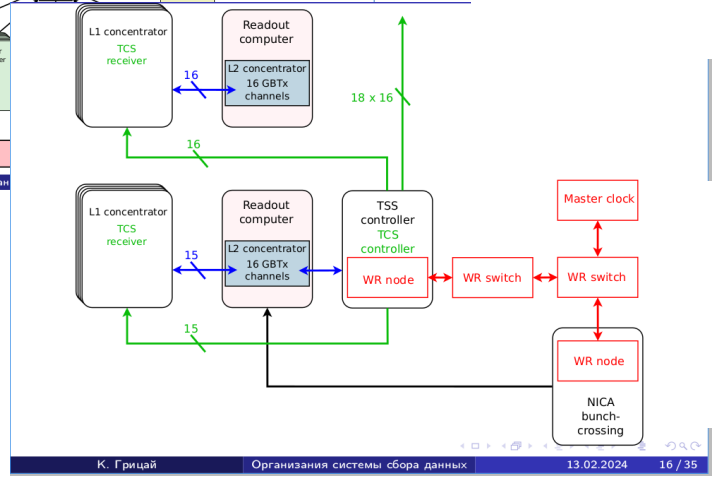
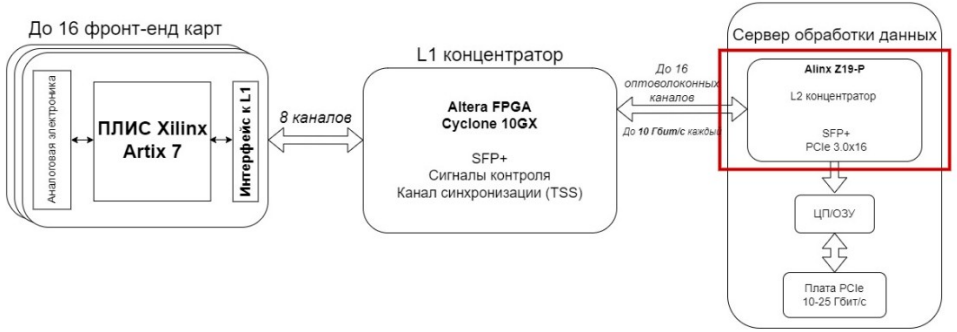
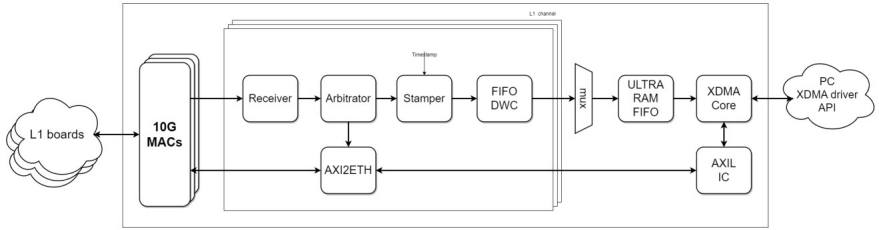
NICA DAQ system

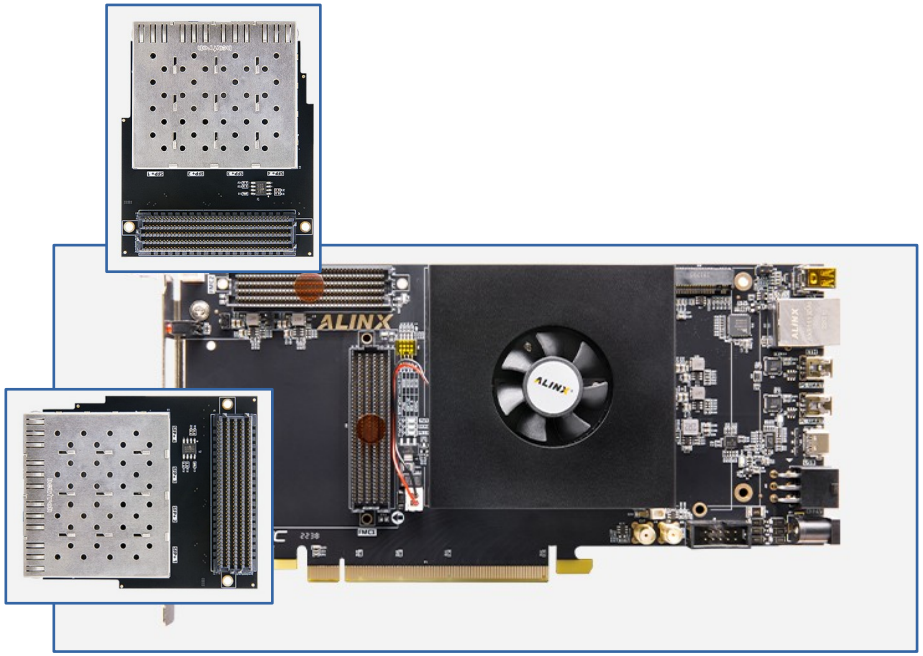






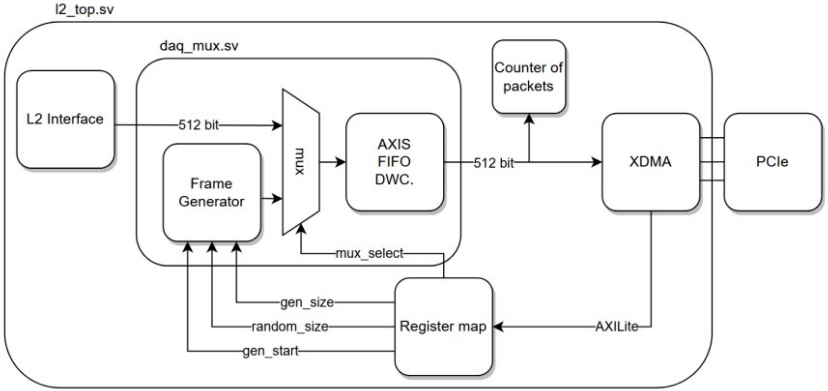


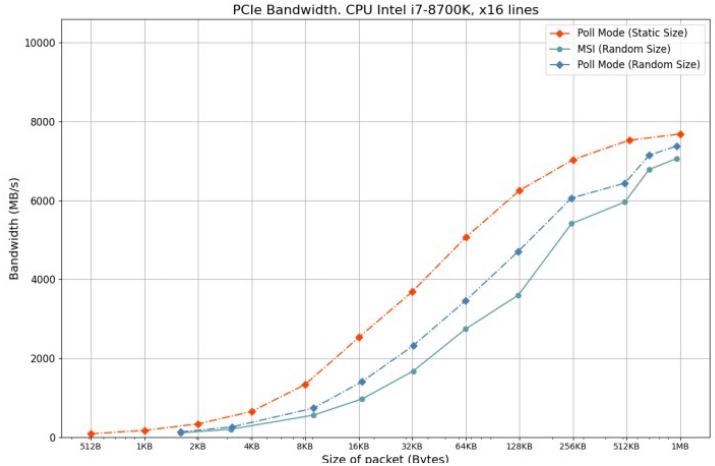
L2 concentrator platform



- Full setup based on Alinx Z19-P board
- Up to 8(16) 10G SFP channels (L1 links/boards)
- PCIe Gen 3.0 x16
- MPSoC XCZU19EG chip

Random-size packets PCIe





Random packets generator in the design

We use it to test and measure performance of PCIe interface

Runtime configuration – controlled by AXILite registers map via DAQ server

MVP for the next stages of DAQ

Data clusterization

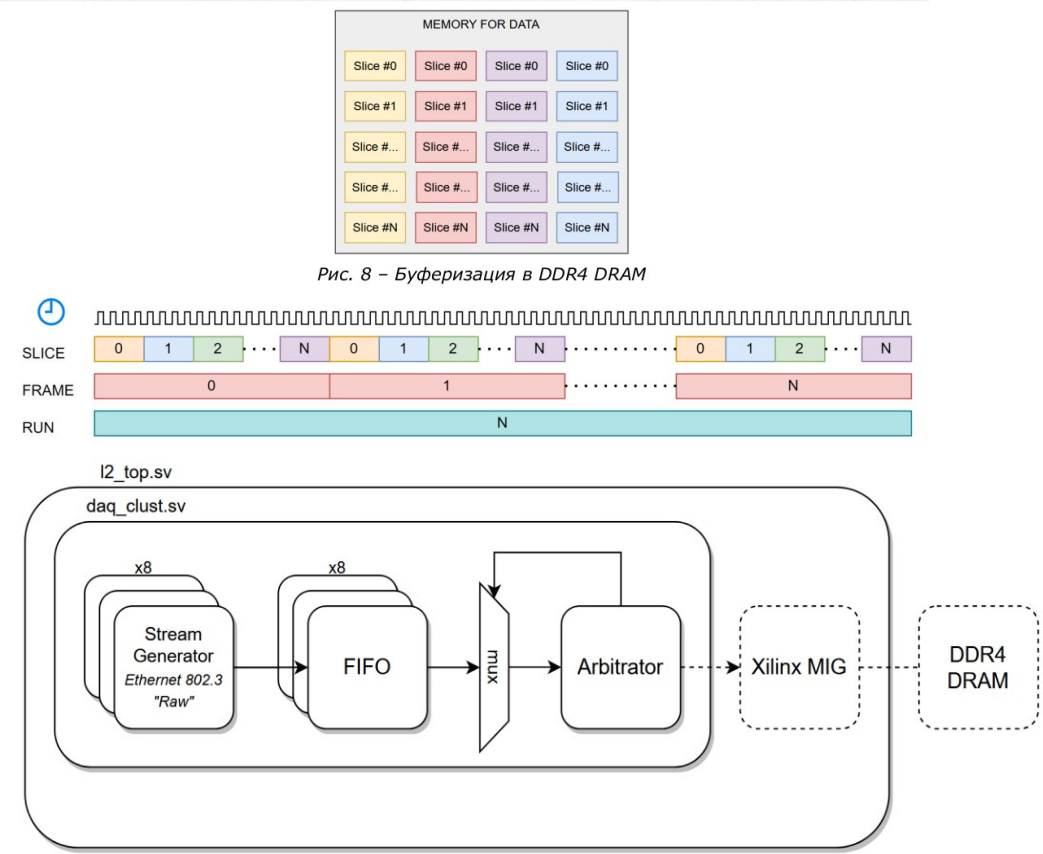


Рис. 8 – Буферизация в DDR4 DRAM

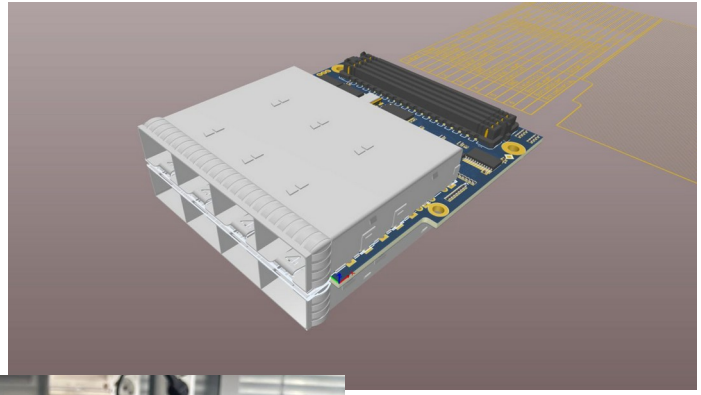
We use onboard PL DDR for data clusterization

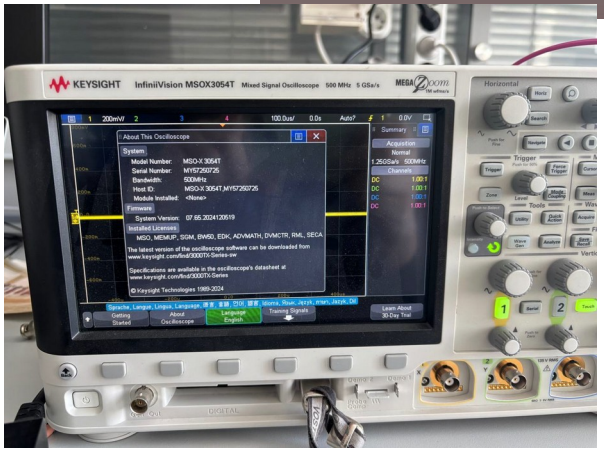
Forward & store input parts of slices into a separate DDR memory locations

Then send them via PCIe to DAQ server

It signifactly improves performance of data transfers. It simplifies first stage data processing @ servers

Hardware activities



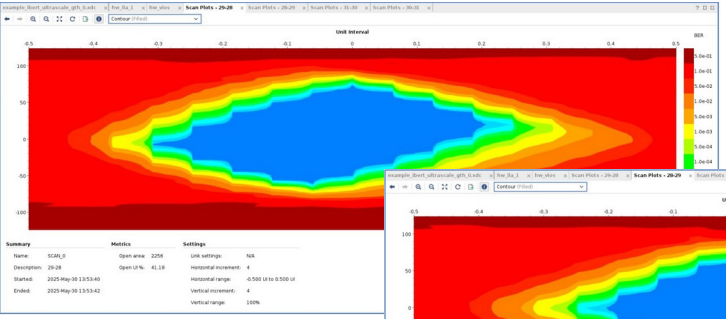


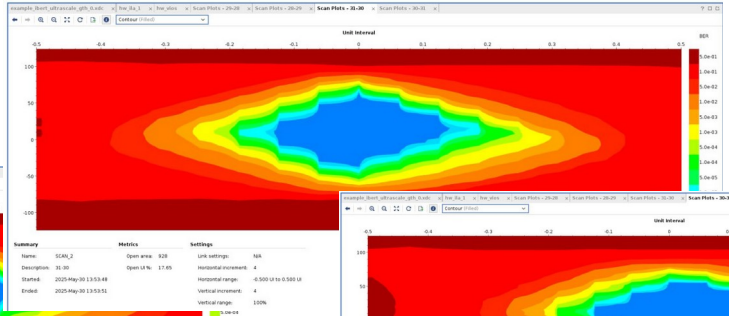
New mezzanine production & assembling confirmed by JINR

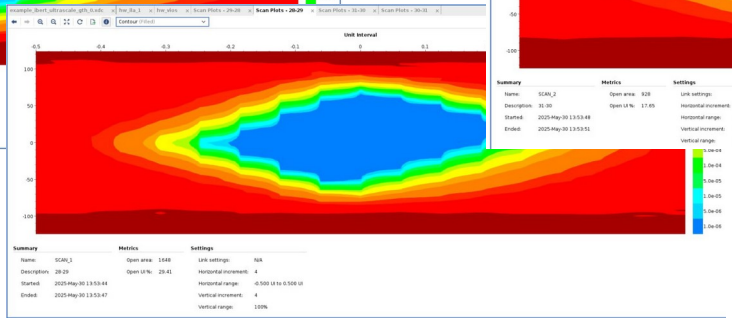
Kirill reflashed our oscilloscope. Now it’s alive

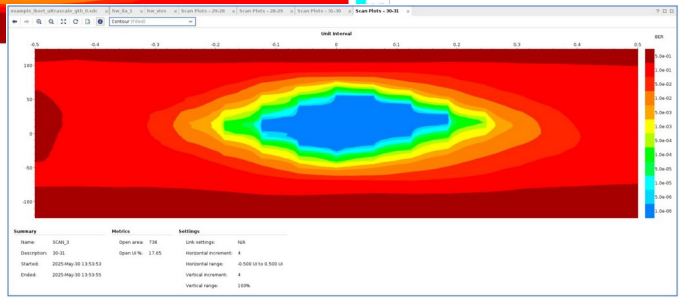
Issues: we observer high BER at 10G Ethernet links on our board**s**. We pushed all the buttons, but the reason is still unclear.

10G issues









Tcl Console | Messages | **Serial I/O Links** | Serial I/O Scans

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PL
Ungrouped Links (0)																		
Found Links (4)							Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	873 mV (11000)	☑	Inject	Reset	Reset		
Auto detected link 0	Quad_231/MGT_X0Y29/TX (xczu19_0)	Quad_231/MGT_X0Y28/RX (xczu19_0)	10.312 Gbps	1.043E12	0E0	9.592E-13	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	873 mV (11000)	☑	Inject	Reset	Reset	Locked	Locke
Auto detected link 1	Quad_231/MGT_X0Y28/TX (xczu19_0)	Quad_231/MGT_X0Y29/RX (xczu19_0)	10.312 Gbps	1.043E12	0E0	9.591E-13	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	873 mV (11000)	☑	Inject	Reset	Reset	Locked	Locke
Auto detected link 2	Quad_231/MGT_X0Y31/TX (xczu19_0)	Quad_231/MGT_X0Y30/RX (xczu19_0)	10.312 Gbps	1.043E12	3.18E2	3.05E-10	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	873 mV (11000)	☑	Inject	Reset	Reset	Locked	Locke
Auto detected link 3	Quad_231/MGT_X0Y30/TX (xczu19_0)	Quad_231/MGT_X0Y31/RX (xczu19_0)	10.307 Gbps	1.043E12	8.9E1	8.536E-11	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	873 mV (11000)	☑	Inject	Reset	Reset	Locked	Locke

Ongoings

- Bringup of clusterization algorithm in simulator;
- Bringup onboard DDR for clusterization data;
- Dima is very close to his Bachelor degree;
- Investigation issues with 10G links: we did a lot, next steps are completely different evaluation board, then new fiber cables, then tests at JINR hardware
- Kirill and Dima on the way to visit to JINR. We prepare drafts of firmware, software and hardware which will be used and improved during visit