National Research Tomsk State University

Laboratory of High Energy Physics Data Analysis
Tomsk State University

Current status of the L2 concentrator development.

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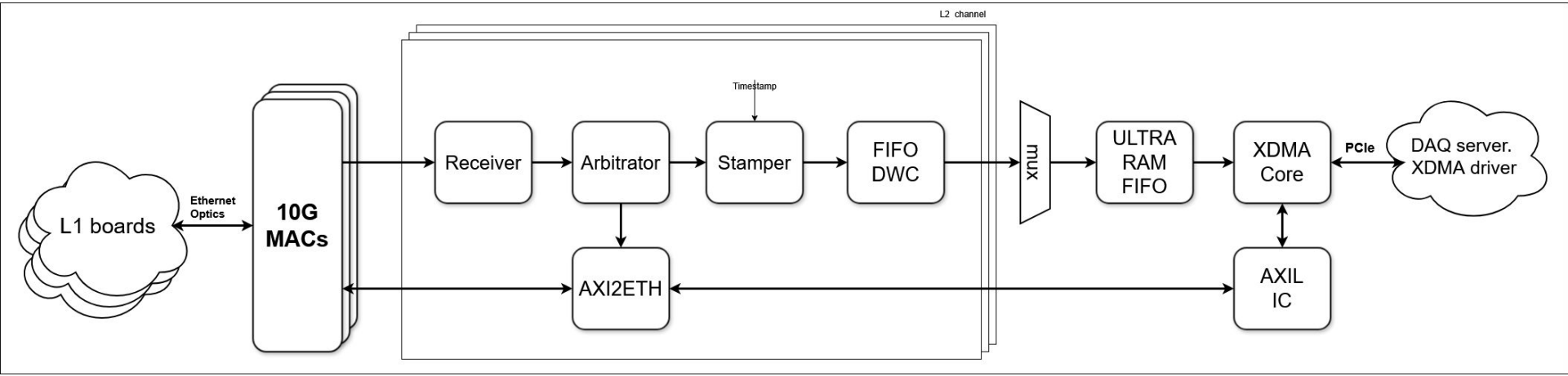
L2 FPGA architecture



All modules are finished.

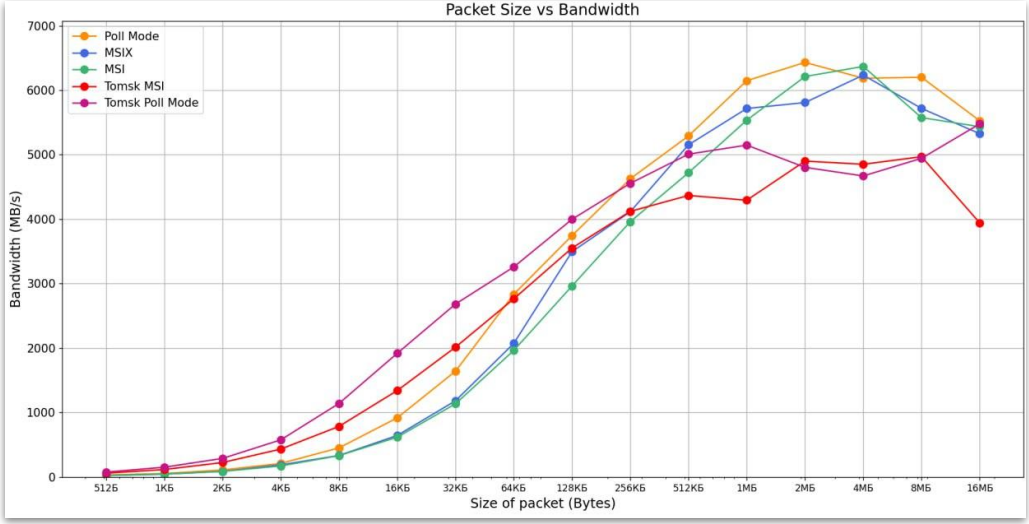
Ethernet channels

The amount of sfp channels in the design is now controlled by a parameter.

In order to achieve better resource management we decided to switch to open-source eth cores.

Currently, we are testing
8 optical Ethernet channels.

DMA Core

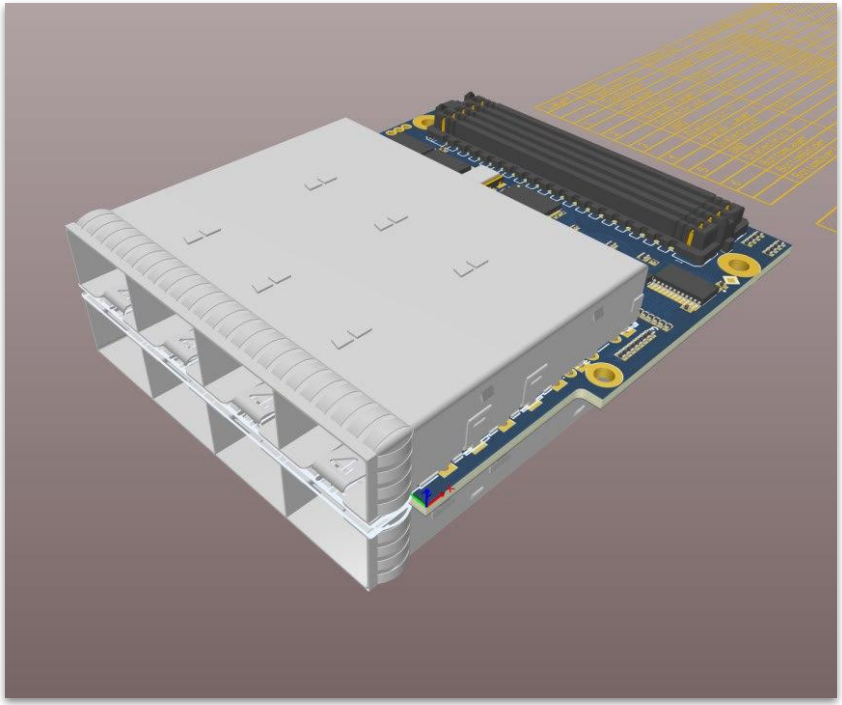


Performance got worse in comparison to tests in Dubna, the reasons are still unknown.

We are thinking of changing DMA core from XDMA to QDMA in the future.

Optimizing algorithms and rewriting the DMA's API to further enhance performance.

New mezzanine card development



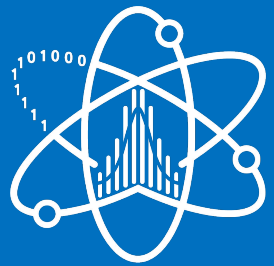
Developed a mezzanine card with 8 SFP+ Channels.

Two prototypes have been ordered for manufacturing.

Ongoing work

1) Transition to other ethernet cores and also testing them.
2) Enhancing algorithms and the DMA's API
3) Optimization of new mezzanine card (we want to make them cheaper).
4) Development of tests using UVM.

Thank you!



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